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CDF SHOWER MAX
SMC CRATE CONTROLLER

Craig Drennan
Fermi National Accelerator Laboratory
PO Box 500, MS222, Batavia, IL 60510
(630) 840-2160, cdrennan@fnal.gov

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I. Introduction

The SMC Crate Controller is installed in Slot 1 of the Shower Max Detector crates and drives all of the control signals on the J1 backplane. The other slots are filled with SMD modules [1] containing the SMQIE Integrators used to digitize charge pulses emanating from Shower Max position detectors on the CDF Central and Plug. Data from all of the SMQIE's on the SMD modules in a crate are transmitted over cables to an SMXR, Shower Max Readout module [2], at the request of the SMXR.

The SMC Crate Controller has four functions. The first is to receive and broadcast the phase adjusted 132 ns clock and the other control signals transmitted from the SMXR. The control signals include the Level 1 Accept and the SMQIE Level 1.5 Write Buffer select bits. There are also Level 1.5 Read Buffer select bits that are latched at the SMC when the Data Transmit Request is received.

The second function is to provide channel select signals that sequence the data out of the SMQIE charge integrators after the Data Transmit Request is received from the SMXR. Four group select address bits are generated that select groups of four SMQIE chips and one of the two channels available on each chip, on each of the SMD modules in the crate. Data from the selected channel of each of the four SMQIE's in a group is referred to as a Quad Set. For each Quad Set it is desired to readout the SMQIE data for either one or four time slices. A time slice is a 132ns integration interval. The SMC generates the time slice bits for the selection of each time slice. The SMC also generates a signal called TRANSMIT that is active for the duration of the data transfer from the SMD modules to the SMXR. This signal is used on the SMD modules to gate the 33 ns data strobe that clocks the data into the SMXR.

The third function of the SMC is to generate a programmable calibration voltage that is referenced by circuits on each SMD module to produce a test current for checking the calibration of the SMQIE's. A sixteen bit data word is written to a precision digital to analog converter. One half of a dual precision op-amp buffers the output voltage of the DAC, while a voltage bias point is buffered with the other op-amp in the package. In this manner the calibration voltage is transmitted differentially to each of the SMD modules.

The fourth and final function of the SMC Crate Controller is to provide diagnostics for the cards in the crate and the SMQIE's in particular. One of the diagnostic functions is the bypass diagnostics mode. In this mode the operator is able to control all of the SMQIE select bits and monitor data coming out of a single channel on each of the SMD modules. This is very usefully in testing and diagnosing the SMQIE's. There are additional diagnostics control signals on the sixty-eight pin control input for this application.

II. Functional Description of the SMC

II.1 The 132ns Beam Clock

In the normal operating mode the 132ns Beam Clock is transmitted from the SMXR Shower Max Readout Board to the SMC over a shielded twisted pair cable using LVDS drivers and receivers. This clock is buffered using a phase-locked loop, and is broadcast by the SMC over the J1 backplane to each of the SMD boards. On the SMD boards it is used as the main system clock for the SMQIE's. Also, on the SMD boards, this clock is multiplied by four using a phase-locked loop to produce a 33ns clock used to strobe the data that is transmitted from the SMD boards to the SMXR. The SMXR is capable of adjusting the phase of the 132ns clock in order to optimize the placement of the SMQIE integration intervals.

The SMC crate controller uses the 132ns clock to drive the sequencer which produces the channel select signals for the SMD boards when a Data Transmit Request has been made.

II.2 Level 1 Accept and SMQIE L1.5 Write Buffer Select Signals

The Level 1 Accept signal is transmitted from the SMXR to the SMC which in turn re-transmits this signal across the J1 backplane to each of the SMD boards. SMQIE L1.5 Write buffer select signals are also transmitted with the Level 1 Accept. These bits inform the SMQIE's on the SMD boards which buffer should be used to store the data, within the SMQIE's, for readout at a later time.

There are some special timing requirements for the Level 1 Accept and the Write buffer select signals with respect to the 132ns clock (as measured at the SMQIE's). The requirements are determined by the SMQIE design. The actual timing is adjusted by the SMXR and some delay logic on the SMC.

The SMC board re-transmits the Write buffer select signals and the shaped Level 1 Accept on the J1 backplane. The SMDI diagnostics computer interface [3] has the capability of emulating all the SMXR signals including the Level 1 Accept and the write buffer select signals.

Note that the shaped Level 1 Accept signal between the SMC and the SMQIE's is an ACTIVE LOW signal. Figure II.2.1 illustrates the signals as seen by the SMQIE.

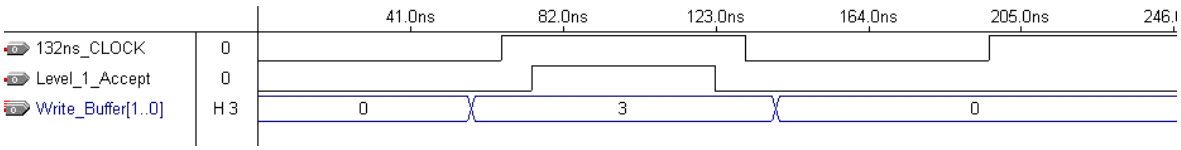

Figure II.2.1 Timing for the Level 1 Accept.

Table II.2.1 Timing parameters for the Level 1 Accept.

Symbol	Parameter	Minimum
Tcs	Clock setup time before Level 1 Accept goes high	> 0 ns
Tch	Clock hold time after Level 1 Accept goes low	> 0 ns
Tds	Write Buffer Select setup time before Clock goes high	5 ns
Tdh	Write Buffer Select hold time after Clock goes low	5 ns
TL1	Level 1 Accept pulse width	20 ns

II.3 Data Transmit Request and SMQIE L1.5 Read Buffer Select Signals

The Data Transmit Request (SMDTR) and the SMQIE L1.5 Read buffer select bits (SMRBUFF[1:0]) are transmitted from the SMXR to the SMC when it is desired to have the SMD boards in the crate transmit the SMQIE data out of the SMD boards to the SMXR. When the SMDTR is found to be high on a rising edge of the 132ns clock the SMC sets a gating signal , TRANSMIT, high and begins sequencing through the time slice select and channel select bits to control the transmission of data out of the SMD boards. The Read buffer select bits are latched on the SMC when SMDTR goes high, and these bits select which L1.5 buffer in the SMQIE's will be transmitted.

II.4 Level 2 Reject

The Level 2 Reject signal is transmitted from the SMXR to the SMC. When the SMC receives this signal data transmission from the SMD boards is immediately halted. The TRANSMIT gate signal is set low and the time slice and channel select line are reset. This signal is not re-transmitted to the SMD boards.

II.5 Mode Select Signals

These signals are transmitted from the SMXR to the SMC. The Mode Select signals, MODESEL[1:0] are decoded on the SMC as follows,

MODESEL[1:0] = 0 -- Normal DAQ Mode.

MODESEL[1:0] = 1 -- Current Injection Enabled.

MODESEL[1:0] = 2 -- Source Monitoring Enabled.

MODESEL[1:0] = 3 -- SMD Electronic I.D. Enabled (PATTEN goes active).

A transition from MODESEL[1:0] = 3 and MODESEL[1:0] = 0 will latch the value on the DIAGADR[5:0] lines to allow the selection of different diagnostic modes described in the SMDI diagnostic interface documentation [3]. The DIAGADR[5:0] lines output from

the SMXR are all pulled High on the SMXR. In this case no diagnostic mode is activated when the MODESEL[1:0] lines transition.

II.6 The Crate and SMQIE Reset Signal

A reset signal, SMRESET, is input through the sixty-eight pin control input connection. The SMC re-transmits the reset signal across the J1 backplane to the SMD boards. The logic on the SMC is reset to a known initial state by this signal, and terminates any transmissions from the SMD boards in the same manner as the Level 2 Reject. The reset is also used to re-initialize the logic on the SMD boards and the SMQIE's. The SMRESET signal is an active high signal. Timing between the SMRESET signal and the 132ns Clock is the same as that between the Level 1 Accept signal and the 132ns Clock.

There is a Power On Reset (POR) generated on the SMC that is OR'ed .with SMRESET. There is also a watchdog timer reset OR'ed with the other two. This will provide a reset to the crate if the 132ns Clock is lost for more than 150ms. The POR and watchdog resets are active for at least 250ms when they do occur.

II.7 The 16-Bit DAC Calibration Voltage Generator

The current injection circuitry on the SMD boards uses a DC reference voltage that is set by a 16-bit DAC on the SMC board. One half of a dual precision op-amp buffers the output voltage of the DAC, while a voltage bias point is buffered with the other op-amp. In this manner the calibration voltage is transmitted differentially to each of the SMD modules across the J1 backplane.

The sixty-eight pin control input connection provides 16 data lines and a data strobe line to allow the DAC to be set by the SMXR or the diagnostics computer. The DAC is an Analog Device's AD669BR, Monolithic 16-Bit DACPORT. The Maxim MAX6225AEPA, Low Noise, Precision, +2.5 V Reference provides the reference voltage for the DAC.. Specifications for these components are reproduced in Table II.7.1 and Table II.7.2. A diagram of the circuit is given in Figure II.7.1.

A design note has been written that considers the possible worst case errors due to inherent non-linearity's and drifts due to changes in temperature. It was determined that if the ambient temperature of the electronics does not vary more than 10 deg F there should be no trouble maintaining a DAC calibration accurate to 13 bits. Measurements on the circuit itself using an oven to vary the ambient temperature have been performed, and have verified this prediction.

The DAC's gain is adjusted by varying the trim input to the +2.5 V reference. In order to maintain a low temperature coefficient, a digital potentiometer part, Dallas DS1869-010, is used instead of a mechanical pot. The digital potentiometer provides better than 15 ppm/degC temperature coefficient for the voltage divider ratio.

The DAC's offset is adjusted by setting DIP switches representing a 16 bit digital bias word. These 16 bits are input to logic including counters within the lower PLD on the SMC. The logic in this PLD adjusts the 16 bit DAC input as it is being loaded from

the SMXR input connection. By this means we do not risk raising the DAC's temperature coefficient and still provide a means of adjusting the DAC's zero output point.

Table II.8.1 MAX6225AEPA, Low Noise, Precision, +2.5 V Reference Specifications.

	Min	Typical	Max	Units
OUTPUT VOLTAGE DRIFT				
+2.5 V Outputs				
0 deg C to +70 deg C		1.0	2.0	ppm / deg C
LINE REGULATION				
Vin = +15 VDC			105	μV / V

Table II.8.2 AD669BR, Monolithic 16-Bit DACPORT Specifications.

	Min	Typical	Max	Units
TRANSFER FUNCTION CHARACTERISTICS				
(-40 deg C to +85 deg C)				
Integral Non-linearity	-1		+1	LSB
Differential Non-linearity	-2		+2	LSB
Unipolar Offset Drift			3	ppm / deg C
Gain Drift (-40 deg C to +85 deg C)	-3		+3	ppm / deg C
Mainly Reference related. Refer to AD688 Output Voltage Drift.				
POWER SUPPLY SENSITIVITY		1	3	ppm / %

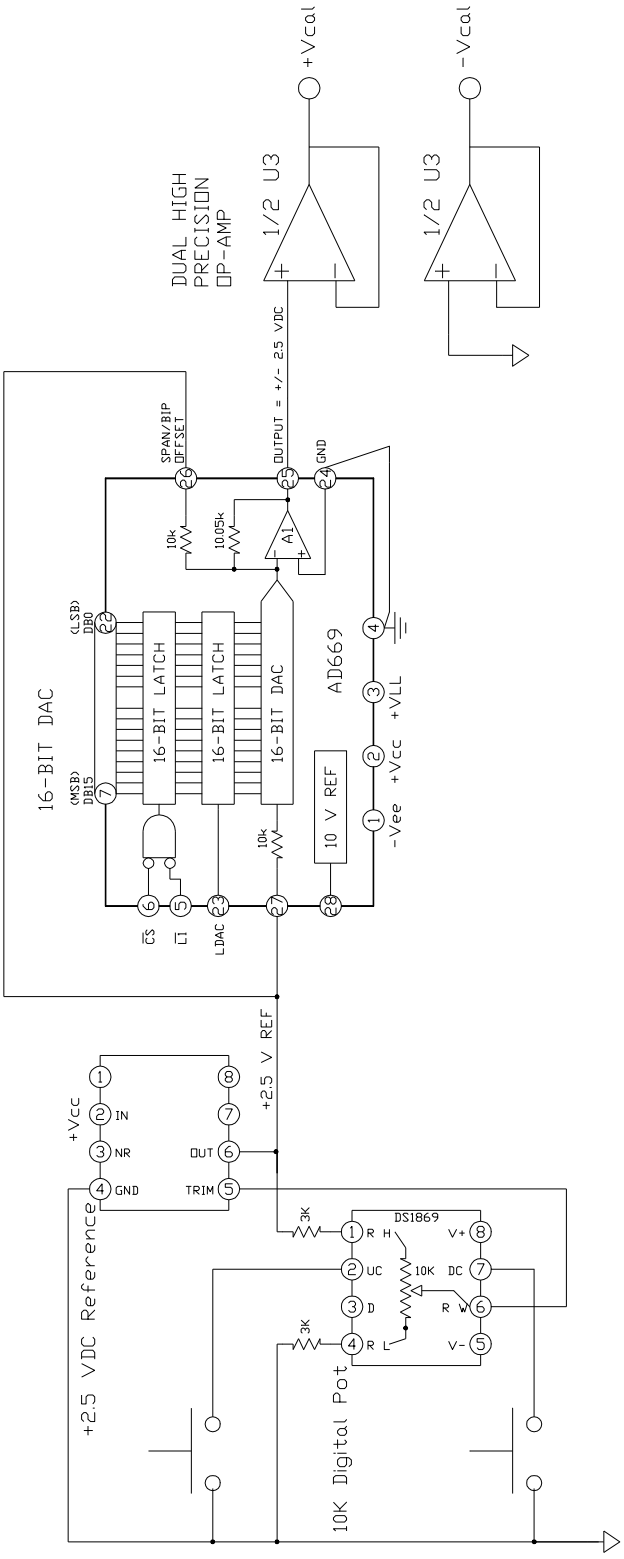

Figure II.8.1. The 16 Bit DAC SMQIE calibration voltage source.

III. Description of the Time Slice and Channel Select Signal Sequencing

The SMC generates the sequence of time slice and channel select signals used by all of the SMD boards in a crate to transmit data from the SMQIE's to the SMXR readout board. There are two types of SMD boards used. The first type is used on the shower max chambers in the Central Calorimeter and has thirty-two SMQIE channels with each channel consisting of four time slices. The second type is used on the phototubes in the Plug Calorimeter and has forty-eight SMQIE channels of one time slice each. The sequencing logic for both types is present in the same PLD and is selectable with a jumper on the SMC.

III.1 Sequence of Select Signals for Thirty-Two Channel SMD Boards

A timing diagram for the sequencing of select signals in a crate of thirty-two channel SMD boards is given in Figure III.1.1.

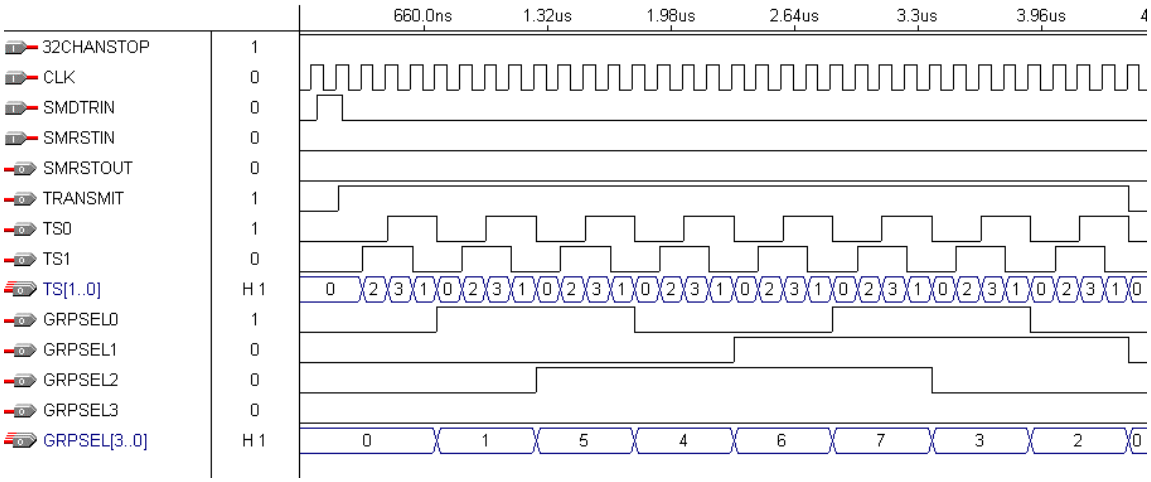

Figure III.1.1 Timing of the select signal sequencing for thirty-two channel SMD boards.

The sequence is started by a high level on the Data Transmit Request line (SMDTRIN) during the rising edge of the 132ns clock (CLK). On the next rising edge of CLK the gate signal TRANSMIT goes high and remains high for the duration of the transmission of data from the SMD boards. This signal is used to gate a 33ns clock on the SMD boards that is used as the data strobe that is sent with the data to the SMXR.

Next, note the time slice select bits TS0 and TS1. From looking at the equivalent binary value of these two bits TS[1..0] it is seen that the time slices are not selected in a straight counting sequence. Rather the bits produce a gray code sequence. This reduces the signal transition frequency and number of simultaneous signal transitions in the signal distribution paths on the backplane and on the SMD boards. This is done to aid in reducing the conducted noise and radiated noise within and out from the crate.

The group select signals, GRPSEL[3..0], are the channel select signals that are also generated in a gray code like sequence. Take note that the SMQIE's are readout four at a time every 132ns. Logic on the SMD boards sequences the four data words selected by the group selects off the board bound for the SMXR at a rate of one word every 33ns. The SMQIE chips are logically arranged into groups of four referred to as Quad Sets. Each chip has two channels that multiplex their data out a single eleven-bit port. The group select signals are decoded on the SMD boards into SMQIE chip selects and SMQIE channel select signals. Table III.1.1 lists some values pertaining to the sequencing of the thirty-two channel SMD boards.

Table III.1.1 Values pertaining to the thirty-two channel SMD boards.

Item	Quantity	Unit
Channels	32	Per SMD board
SMQIE Chips	16	Per SMD board
Quad Sets	8	Per SMD board
Groups	8	Per SMD board
Data words transmitted per cycle	128	Per SMD board
Duration of transmit cycle	4.224	us
Period of Time Slice Bits	528	ns
Transition rate. of TS[1..0] Bits	7.576e6	Transitions / Second
Avg. Transition rate of GRPSEL[3..0]	1.894e6	Transitions / Second

III.2 Sequence of Select Signals for Forty-Eight Channel SMD Boards

A timing diagram for the sequencing of select signals in a crate of forty-eight channel SMD boards is given in Figure III.2.1. This version requires that only one time slice be transmitted for each SMQIE channel. Therefore, you see that the time slice bits remain fixed throughout the cycle and that the group select bits change every 132ns. A table of pertinent values like those given for the thirty-two channel boards is listed in Table III.2.1 for comparison.

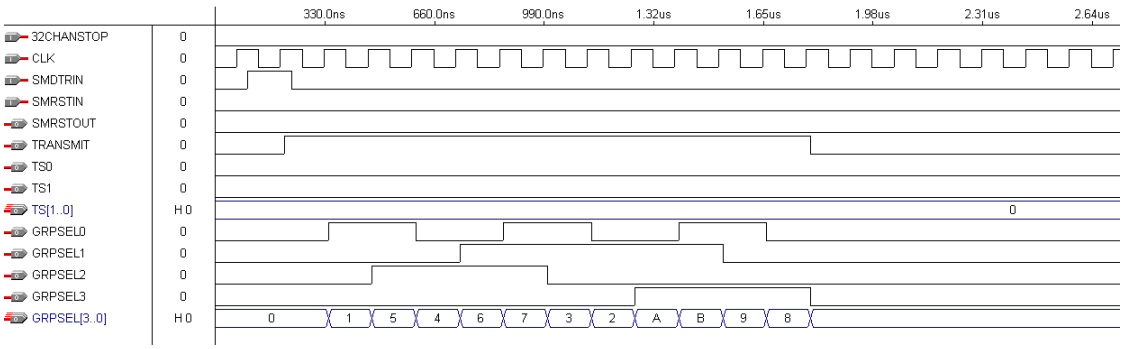

Figure III.2.1 Timing of the select signal sequencing for forty-eight channel SMD boards.

Table III.2.1 Values pertaining to the forty-eight channel SMD boards.

Item	Quantity	Unit
Channels	48	Per SMD board
SMQIE Chips	24	Per SMD board
Quad Sets	12	Per SMD board
Groups	12	Per SMD board
Data words transmitted per cycle	48	Per SMD board
Duration of transmit cycle	1.584	us
Period of Time Slice Bits	---	ns
Transition rate. of TS[1..0] Bits	0	Transitions / Second
Avg. Transition rate of GRPSEL[3..0]	7.576e6	Transitions / Second

IV. The SMXR to SMC Control Link

The 132ns clock, Level 1 Accept and other control signals for the SMD crate are transmitted from the SMXR to the SMC Crate Controller over the SMXR to SMC Control Link.

IV.1 Components of the SMXR to SMC Control Link

The control link between the SMXR and the SMC uses LVDS drivers and receivers connected with a shielded thirty-four twisted pair cable. One end of the cable is connected to a transition card in the rear of the VME crate, in a slot behind the SMXR driving the signals on the cable. The other end of the cable is connected to the sixty-eight-pin control input connector on the front panel of the SMC. The specific part numbers for the cable, connectors and LVDS driver and receiver are given in Table IV.1.1. The pin assignment for the connection is given in Table IV.1.2.

LVDS stands for Low Voltage Differential Signaling. This is a relatively new technology that has the advantages lower power consumption and smaller signal swings (hence, lower EMI). It is also capable of high data rates and is used in the general market for high-speed SCI links and video display links in laptop computers. The DS90C031 differential line driver is a balance current source design. The typical output current is 3.45 mA, a minimum current of 2.5 mA, and a maximum of 4.5 mA. The 3.45 mA loop current will develop a differential voltage of 345 mV across the 100 Ohm termination resistor which the receiver detects with a 245 mV minimum differential noise margin. The signal is centered around 1.2 V with respect to ground. The total signal swing is typically 690 mV.

Table IV.1.1 SMXR to SMC Control Link Components.

Item	Manufacturer	Part #	Description
1	3M	3600B/68	68 conductor, 28 AWG stranded, twisted pair, PVC/PVC, aluminum film foil and copper braid overall shield.
2	3M	10268-55H3VC	Connector, 0.050” pitch, board mount, right angle, 68 position receptacle.
3	3M	10168-6000EC	.050” wire mount plug.
4	3M	10368-3210-000-1	Plastic junction shell, internal metal EMI shell.
5	National	DS90C031TM	Quad LVDS driver.
6	National	DS90C032TM	Quad LVDS receiver.

Table IV.1.2. Pin Assignments for the SMXR to SMC Link

Pin #	Signal Name	Description
1. 35.	SMCLK+ SMCLK-	132 ns Beam Clock for SMQIE's and generation of the transmit data strobe on the SMD boards.
2. 36.	SMRST+ SMRST-	Reset signal for the SMQIE's and other control logic.
3. 37.	SML1A+ SML1A-	Level 1 Trigger Accept is used as a WRITE pulse to write data emerging from the end of the Level 1 pipeline inside the SMQIE's to be written into the Level 1.5 buffer specified by SMWB[1:0].
4. 38.	SMDTR+ SMDTR-	SMXR request to begin data transfer from the SMD SMQIE's.
5. 39. 6. 40.	SMWB1+ SMWB1- SMWB0+ SMWB0-	Write SMQIE data buffer number for L1.5.
7. 41. 8. 42.	SMRB1+ SMRB1- SMRB0+ SMRB0-	Read SMQIE data buffer number for L1.5.
9. 43. 10. 44.	MODESEL0+ MODESEL0- MODESEL1+ MODESEL1-	The mode select signals set by the SMXR or diagnostics computer. MODESEL[1:0] = 0 -- Normal DAQ Mode. MODESEL[1:0] = 1 -- Current Injection Enabled. MODESEL[1:0] = 2 -- Source Monitoring Enabled. MODESEL[1:0] = 3 -- SMD Electronic ID Enabled (PATTEN).
11. 45.	SML2R+ SML2R-	Level 2 Reject signal that halts SMD transmission cycle immediately to make Level 1.5 buffers available.
12. 46.	SMSTRB+ SMSTRB-	Data strobe for SMDATA[15:0].
13. 47. o o o 28. 62.	SMDATA15+ SMDATA15- o o o SMDATA0+ SMDATA0-	Input data word for the 16-bit DAC that generates the calibration voltage for the SMQIE's
29.	DIAGADR0+	The diagnostic address select bits are used in the bypass diagnostics mode to select a specific SMQIE channel on the SMD boards for

63. o o o 34. 68.	DIAGADR0- o o o DIAGADR5+ DIAGADR5-	monitoring. The upper four bits, DIAGADR[5:2], replace GRPEN[3:0] that are normally generated by the sequencer on the SMC to select the specific set of four SMQIE's and one of the two channels on each of them. That is they select a specific Quad Set of data. The lower two bits, DIAGADR[1:0] control the DIAG_OE_SEL[1:0] bits sent across the backplane that select one of the four data words of the Quad Set.

IV.2 Termination of the SMXR to SMC Control Link

The termination of the common mode component of the signals on the cable, as well as the differential component was considered essential in the effort to keep radiated noise from the cable to a minimum. The termination scheme is illustrated in Figure IV.2.1. Note the termination for the differential signal is split into two equal value resistors so the node between them can be considered to be at the common mode voltage potential. It is between this node and ground that the common mode is AC terminated.

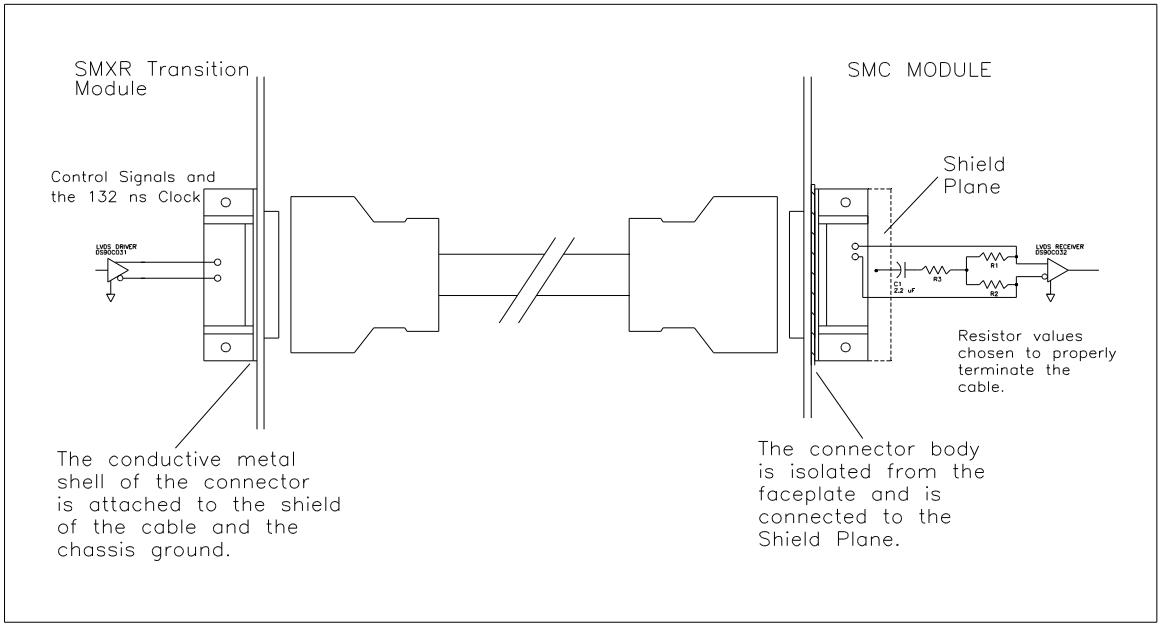

Figure IV.2.1 Termination of the SMXR to SMD control link.

V. Signal Transmission on the J1 Backplane

The backplane used in the crate is a standard VME J1 backplane. We are not using any of the signals defined in the VME specification, but the backplanes are available off-the-shelf. The backplane in the crate is Schroff Part # 23030-175. The SMC Crate Controller is installed in the first slot and is the only card in the crate that drives data onto the backplane. In the last slot of the crate is a board that provides the

termination for the backplane. The only other cards in the crate are the SMD boards. There are no more than eight SMD boards in a crate.

V.1 Signals Assigned to the Backplane

All of the signals on the backplane utilize the LVDS technology. It was determined that this would provide for the least amount of radiated noise from the crate. In order to use a backplane that was readily available off-the-shelf, how a particular manufacturer laid out the traces and signal layer had to be considered since the LVDS signals are differential. In order to avoid excessive crosstalk and benefit from the external electromagnetic field cancellation effect of differential signaling, the two signal traces for each of the differential signals needed to be adjacent. They could not be separated by other signal traces, or a power or ground plane. Hence, in assigning signals to the backplane, connections were not assigned according to which connector pin was adjacent to another, but rather according to which connector pins were connected to traces on the backplane that were adjacent to one another. The resulting signal assignment is given in Table V.1.1. A description of the signals in this table is given in Table V.2.1.

Table V.1.1. SMD backplane signal connector pin assignments.

Pin #	Row A	Row B	Row C
1	G	SMCALEN1+	G
2	SMCALEN1-	SMCALEN2+	G
3	SMCALEN2-	PATTEN+	G
4	PATTEN -	G	G
5	ONECHEN+	G	ONECHEN -
6	G	G	G
7	SMRST+	G	SMRST-
8	G	G	G
9	G	G	G
10	DIAG_OE2+	G	DIAG_OE2-
11	G	G	G
12	DIAG_OE3+	ONECHSEL1+	DIAG_OE3-
13	ONECHSEL1-	ONECHSEL0+	TRANSMIT+
14	ONECHSEL0-	TRANSMIT-	SML1A+
15	G	SML1A-	SMRB1+
16	G	SMRB1-	SMRB0+
17	G	SMRB0-	SMWB1+
18	G	SMBW1-	SMWB0+
19	G	SMBW0-	G
20	G	G	SMVCAL+
21	G	SMVCAL-	G
22	G	GRPSEL3+	G
23	GRPSEL3-	G	GRPSEL2+
24	G	GRPSEL2-	GRPSEL1+
25	G	GRPSEL1-	GRPSEL0+
26	G	GRPSEL0-	TS1+
27	G	TS1-	TS0+
28	G	TS0-	SMCLK+
29	-15VDCMON	SMCLK-	+15VDCMON
30	G	AGNDMON	G
31			
32	+5VDC (VCC)	+5VDC (VCC)	+5VDC (VCC)

Table V.1.2 SMD signal descriptions

Signal Name	Description
SMCLK	132 ns Beam Clock for SMQIE's and generation of the transmit data strobe.
SMRST	Reset signal for the SMQIE's and other control logic.
SML1A	Level 1 Trigger Accept is used as a WRITE pulse to write data emerging from the end of the Level 1 pipeline inside the SMQIE's to be written into the Level 1.5 buffer specified by SMWB[1:0].
SMWB[1:0]	Write SMQIE data buffer number for L1.5.
SMRB[1:0]	Read SMQIE data buffer number for L1.5.
SMCALEN1	Calibration enable signal which enables the DC current injection circuitry to calibrate the ranges and phases of the SMQIE.
SMCALEN2	Calibration enable signal which enables the source monitoring circuitry needed by the Plug Shower Max.
SMVCAL	Differential DC calibration voltage used to set the calibration current for the SMQIE's.
TS[1:0]	The Time Slice select bits control the SMQIE TS[1:0] pins to select which Time Slice will be readout.
GRPSEL[3:0]	The Group Select bits are decoded into chip enables and channel select lines for accessing data in the SMQIE's.
TRANSMIT	Used by logic on each SMD Board to gate the Data Strobe (33 MHz clock) and other sequencing on the SMD boards.
ONECHSEL[1:0]	These output enables are used by the crate diagnostics to select one of the four 11 bit data words from a particular Quad Set. The output enables used during normal data transfer are derived on each SMD board. The ONECHEN signal is used to switch between the use of these two sources. Currently ONECHSEL[1:0] are decoded on the SMD boards to produce the four output enables needed.
DIAG_OE_SEL[3:2]	DIAG_OE_SEL[3:2].are currently not used.
ONECHEN	Enables the One Channel select mode.
PATTEN	Pattern Diagnostics enable signal.
+15VDCMON	This is a connection to the +15VDC used for the DAC on the SMC. This is used for voltage monitoring on the Termination board at the other end of the crate. The +15VDC is supplied to the SMC through a transition card tied to J2.
-15VDCMON	This is a connection to the -15VDC used for the DAC on the SMC. This is used for voltage monitoring on the Termination board at the other end of the crate. The -15VDC is supplied to the SMC through a transition card tied to J2.
AGNDMON	This is a connection to the Analog Ground used for the DAC on the SMC. This is used for voltage monitoring on the Termination board at the end of the other end of the crate
G	This is a ground connection made on the SMC board. No connection to these pins are made on the SMD boards.

V.2 Termination of LVDS Signals on the Backplane

An issue that had to be addressed when deciding to use LVDS signals across the J1 backplane. Early tests of the LVDS signals across the Schroff VME J1/P1 backplane indicated that capacitive loading of the bus with ten of the receiver boards installed resulted in marginal switching characteristics of the LVDS signals. When the bus was terminated with the typical 100 Ohms specified for the LVDS receiver the signal had a pronounced " stair-step" transition caused by the mismatch of the signal transmission line impedance and the termination. When terminated in the transmission line impedance the signal swing was just barely within the worst case switching thresholds for the DS90C032 LVDS receiver (+/- 100 mV).

Steps were taken to reduce the capacitance of each LVDS receiver board as seen by the backplane. With a careful choice of termination of the differential signals (approx. 71 Ohms) on the card in the last slot of the crate, and by employing the technique of AC termination of the common mode signal, clean signal transitions of +/- 200 mV are achieved

VI. Diagnostics

VI.1 Setting Diagnostic Modes

There are currently six diagnostic modes that are implemented for the SMD crate electronics. These modes are enabled and disabled using the DIAGADR[5:0] and MODESEL[1:0] signals. A description of each diagnostic mode and how it is enabled is given in the following sections. All of the diagnostic modes are settable using the SMDI Shower Max Diagnostic Interface connected to a PC. Only the PATTEN diagnostics mode can be set online using the SMXR.

VI.2 The SMD Digitizer, PATTEN Diagnostics Mode

In this mode the SMD digitizer boards will output a predetermined sequence out its SMD to SMXR Data port. This sequence includes a unique identification number for the SMD board, and an indication of the functionality of the chip select sequencing that originates on the SMC. A detailed description of the PATTEN diagnostic output is provided in the documentation for the SMD Digitizer board [1].

The PATTEN diagnostics mode is enabled by having DIAGADR[5:0] set all high or all low and then having both MODESEL0 and MODESEL1 go high. The PATTEN bit on the backplane is set active at this point. The PATTEN diagnostic mode is disabled whenever one or both of MODESEL0 and MODESEL1 are low.

VI.3 The 32 Channel Diagnostics Mode

In this mode the SMC is forced to provide SMQIE chip select sequences that are used with the 32 channel SMD boards, independent of the jumper setting on the SMC. This is used mainly in the production checkout or troubleshooting of the SMC boards.

The 32 Channel diagnostics mode is enabled by having DIAGADR[5:0] set equal to 0x05 or 0x3D (hexadecimal) and then having both MODESEL0 and MODESEL1 go high. The DIAGADR[5:0] signals are latched when both MODESEL0 and MODESEL1 go high. This allows the MODESEL bits to be used to enable the current injection calibration or source monitoring. The 32 Channel diagnostic mode is disabled by having DIAGADR[5:0] set equal to 0x00 or 0x3F (hexadecimal) and then having both MODESEL0 and MODESEL1 go high once again. Note that it is the transition of MODESEL[1:0] that clocks in the value set on DIAGADR[5:0] .

VI.4 The 48 Channel Diagnostics Mode

In this mode the SMC is forced to provide SMQIE chip select sequences that are used with the 48 channel SMD boards, independent of the jumper setting on the SMC. This is used mainly in the production checkout or troubleshooting of the SMC boards.

The 48 Channel diagnostics mode is enabled by having DIAGADR[5:0] set equal to 0x06 or 0x3E (hexadecimal) and then having both MODESEL0 and MODESEL1 go high. The DIAGADR[5:0] signals are latched when both MODESEL0 and MODESEL1 go high. This allows the MODESEL bits to be used to enable the current injection calibration or source monitoring. The 48 Channel diagnostic mode is disabled by having DIAGADR[5:0] set equal to 0x00 or 0x3F (hexadecimal) and then having both MODESEL0 and MODESEL1 go high once again. Note that it is the transition of MODESEL[1:0] that clocks in the value set on DIAGADR[5:0] .

VI.5 The Alternate Diagnostic Port Diagnostics Mode

In this mode the SMC is switches signals that are not normally observable on the 26 pin diagnostics port on the SMC to replace the ones that are. This is used mainly in the production checkout or troubleshooting of the SMC boards. Table VI.5.1 lists the signals that normally appear on the 26 pin diagnostics port and the alternate signals that appear in this diagnostic mode.

Table VI.5.1 SMC Diagnostic Port re-assignments.

Signal	Normal Mode	Alternate Diagnostic Mode
1	L1A, as seen on backplane	SML1A, as seen from SMXR
2	TS0	DIAGADR0
3	TS1	DIAGADR1
4	GRPSEL0	DIAGADR2
5	GRPSEL1	DIAGADR3
6	GRPSEL2	DIAGADR4
7	GRPSEL3	DIAGADR5
8	WB0	MODESEL0
9	WB1	MODESEL1
10	RB0	SML2R
11	RB1	SMRESET
12	TRANSMIT	(Held LOW)
13	132ns CLOCK	132ns CLOCK

The Alternate Diagnostic Port diagnostics mode is enabled by having DIAGADR[5:0] set equal to 0x04 or 0x3C (hexadecimal) and then having both MODESEL0 and MODESEL1 go high. This diagnostic mode is disabled by having DIAGADR[5:0] set equal to 0x00 or 0x3F (hexadecimal) and then having both MODESEL0 and MODESEL1 go high once again. Note that it is the transition of MODESEL[1:0] that clocks in the value set on DIAGADR[5:0] .

VI.6 The Single Channel Diagnostics Mode

In this mode the SMC activates the ONECHEN signal on the backplane causing the SMD Digitizer Boards to go into their single channel mode. Once in the Single Channel mode the DIAGADR[5:0] signals coming into the SMC control SMQIE channel selection. Table VI.6.1 indicates which signals are controlled by the DIAGADR[5:0] signals. The ONECHEN signal's activation causes the SMD Digitizer boards to use the ONECHSEL[1:0] signals to select one of four of the signals of a "Quad Set" selected by the GRPSEL[3:0] signals, instead of its normal multiplexing. In this manner the SMD will fill a normal data transmission with a single channels data in response to a Data Transmit Request. Note that the Time Slice bits TS[1:0] are not effected and transition as normal. Therefore in a 32 channel system the four time slices are repeatedly transmitted in the Single Channel diagnostics mode.

Table VI.6.1 Single Channel chip selection control.

SMC Control Input	SMD Backplane Input
DIAGADR0	ONECHSEL0
DIAGADR1	ONECHSEL1
DIAGADR2	GRPSEL0
DIAGADR3	GRPSEL1
DIAGADR4	GRPSEL2
DIAGADR5	GRPSEL3

The Single Channel diagnostics mode is enabled by having DIAGADR[5:0] set equal to 0x03 or 0x3B (hexadecimal) and then having both MODESEL0 and MODESEL1 go high. This diagnostic mode is disabled by having DIAGADR[5:0] set equal to 0x00 or 0x3F (hexadecimal) and then having both MODESEL0 and MODESEL1 go high once again. Note that it is the transition of MODESEL[1:0] that clocks in the value set on DIAGADR[5:0] .

VI.7 The Bypass Diagnostics Mode

The Bypass diagnostics mode operates just like the Single Channel mode except that the Time Slice bits TS[1:0], the Read Buffer bits SMRB[1:0], and the Write Buffer bits SMWB[1:0] are all set low. Also the TRANSMIT signal is continuously active (high) and the L1A signal is replaced by the 132ns Clock. By continuously clocking the SMQIE L1A pin data is continuously being written into the Write Buffers. By setting the TRANSMIT signal active data is continuously being read from the chosen channel and being transmitted out the SMXR Data port.